BRIEF DESCRIPTION OF THE DRAWINGS

A better understanding of the present invention can be obtained when the following detailed description is considered in conjunction with the following drawings, in which:

Figure 1 illustrates a multiple chip module configured in accordance with the present invention;

Figure 2 illustrates a traditional pin assignment;

Figure 3 illustrates a pin assignment with a triangular pattern that reduces the lengths of orthogonal interconnections in accordance with the present invention;

Figure 4 illustrates an embodiment of the present invention of a multiple chip module with pins used for diagonal interconnections assigned in a triangular pattern;

Figure 5 illustrates an embodiment of the present invention of a computer system;

Figure 6 is a flowchart of a method for identifying pin locations to be used for diagonal interconnections; and

Figures ~~7~~ 7A-7D illustrates a spreadsheet used to identify pin locations on a chip in a multiple chip module that should be used for diagonal or orthogonal signal pins.

Implementations of the invention include implementations as a computer system programmed to execute the method or methods described herein and as a computer program product. According to the computer system implementations, sets of instructions for executing the method or methods may be resident in the RAM 514 of one or more computer systems configured generally as described above. Until required by computer system 500, the set of instructions may be stored as a computer program product in another computer memory, for example, in disk unit 520. Furthermore, the computer program product may also be stored at another computer and transmitted when desired to the user's workstation by a network or by an external network such as the Internet. One skilled in the art would appreciate that the physical storage of the sets of instructions physically changes the medium upon which it is stored so that the medium carries computer readable information. The change may be electrical, magnetic, chemical or some other physical change.

<u>Figure 6 - Method for Identifying Pin Locations to be Used for Diagonal Interconnections</u>

Figure 6 is a flowchart of one embodiment of the present invention of a method 600 for identifying pin locations in chip 110 (Figure 1) to be used for diagonal interconnections. Method 600 will be discussed in conjunction with Figures 7A-7D depicting a spreadsheet 700 illustrating the calculated lengths of the orthogonal and diagonal interconnections as well as which particular pins are to be used for diagonal interconnections determined in accordance with the present inventive principles as explained in greater detail further below. It is noted that Figures ~~7~~ 7A-7D are ~~is~~ illustrative and ~~is~~ are not to be construed in a limiting manner.

Referring to Figure 6, in conjunction with Figures 4 and 7, in step 601, the lengths of a plurality of orthogonal interconnections from a particular chip 110, e.g., chip 110A, to an adjacent chip 110, e.g., chip 110B, may be calculated. Referring to Figures ~~7~~ 7A-7B, a row 701 of orthogonal values, which may represent the length of

orthogonal interconnections, thus calculated, where the values 702A-P represent distances in millimeters from pins in corresponding row/column combinations in adjacent chips 110. For example, the first value 702A in row 701 may refer to the distance between the pin position in chip 110, e.g., chip 110A, at row 451A/column 471 with the corresponding pin position in the adjacent chip 110, e.g., chip 110B. The first value may be a zero value because lengths in Figure 7 A may be differential distances relative to the first length value. The second value 702B in row 701 may refer to the differential distance between the pin position in chip 110, e.g., chip 110A, at row 451B/column 471 with the corresponding pin in the adjacent chip 110, e.g., chip 110B, and so forth. The second value 702B, e.g., .8007 millimeters, may represent the additional distance in length to the first value length. It is noted that value 702P in row 701 represents the longest differential orthogonal distance, e.g., 12.0102 millimeters, between the pin position in chip 110, e.g., chip 110A, at row 451P/column 171 and the corresponding pin in the adjacent chip 110, e.g., chip 110B. It is further noted that the orthogonal distances may be calculated using any column of adjacent chips 110 and that the above is illustrative. It is further noted that some of the values in row 701, e.g., value 702E, may refer to the differential distance between a pin position reserved for non-connecting purposes, e.g., power, ground, in chip 110, e.g., row 451E, column 471 in chip 110A, with the corresponding pin in the adjacent chip 110, e.g., chip 110B.

In step 602, the lengths of a plurality of diagonal interconnections from a particular chip 110, e.g., chip 110A, to a diagonal chip 110, e.g., chip 110C, may be calculated. Referring to Figure 7, spreadsheet 700 comprises rows 703A-N, where N may be any number, and columns labeled "A-P" used to indicate the lengths of calculated diagonal interconnections between diagonal chips 110. Rows 703A-N may collectively or individually be referred to as rows 703 or row 703, respectively. Each particular row/column combination may represent a particular pin location on a particular chip 110, e.g., chip 110A. Further, each particular row/column

combination may comprise a value for a length of a particular diagonal interconnection. The value may represent the differential distance in millimeters with respect to the shortest orthogonal distance. That is, the value in each particular row/column combination in spreadsheet 700 may represent the length of a particular diagonal interconnection in millimeters that is additional to value 702A. (It is noted that the zero value for the differential distance in row 703A has been suppressed in Figure 7 because the corresponding pin located at row 451A/column 461A is reserved for non-connecting purposes.) For example, the value, e.g., .2003 millimeters, at row 703B/column "A" may refer to the additional distance in length to value 702A between the pin position in chip 110, e.g., chip 110A, at row 451B/column 461A with the corresponding pin in the diagonal chip 110, e.g., chip 110C. The value, e.g., .601 millimeters, at row 703C/column "A" may refer to the additional distance in length to value 702A between the pin position in chip 110, e.g., chip 110A, at row 451C/ column 461A with the corresponding pin in the diagonal chip 110, e.g., chip 110C. The value, e.g., 1.0017 millimeters, at row 703D/column "A" may refer to the additional distance in length to value 702A between the pin position reserved for non-connecting purposes, e.g., power, ground, in chip 110, e.g., chip 110A, at row 451D/ column 461A with the corresponding reserved pin position in the diagonal chip 110, e.g., chip 110C, and so forth. Hence, the values in rows 703 for each column may represent the value of the differential distance between the pin position in chip 110, e.g., chip 110A, at various rows 451 for a particular column 461 with the corresponding pin in the diagonal chip 110, e.g., chip 110C. The values in columns for each row 703 may represent the value of the differential distance between the pin position in chip 110, e.g., chip 110A, at various columns 461 for a particular row 451 with the corresponding pin in the diagonal chip 110, e.g., chip 110C, as described below.

The value in row 703C/column "B" may refer to the differential distance between the pin position in chip 110, e.g., chip 110A, at row 451C/column 461B with